Electronic Version
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Claims

[c1] 1.A thin film transistor, comprising:
a gate electrode, formed on a substrate, wherein the gate electrode has at least one notch;
a gate dielectric layer, formed over the substrate, covering the gate electrode;
a source region, formed on the gate dielectric layer, wherein the source region is located over a region outside the notch of the gate electrode and the source region overlaps a portion of the gate electrode;
a drain region, formed over the gate dielectric layer exposed by the source region, wherein the drain region is over the notch of the gate electrode and the drain region overlaps a portion of the gate electrode at the edge of the notch; and
a channel layer formed on the gate dielectric layer and located over the gate electrode and between the source region and drain region.

[c2] 2. The thin film transistor of claim 1, further comprising an etch stop layer formed between the channel layer and the source and drain regions.

[c3] 3. The thin film transistor of claim 1, further comprising

an ohmic-contact layer formed between the channel layer and the source and drain regions.

[c4] 4. The thin film transistor of claim 1, wherein the source region overlaps the gate electrode.

[c5] 5. The thin film transistor of claim 1, wherein the source region comprises two strip regions, each of the two strip regions adjacent to each longitude of the drain region.

[c6] 6. The thin film transistor of claim 1, wherein the shape of the notch of the gate electrode is a triangle, a quadrilateral or a non-regular shape.

[c7] 7. A pixel structure, comprising:
a scan line, formed on a substrate;
a gate electrode, formed on the substrate and electrically connected to the scan line, wherein the gate electrode has at least one notch;
a gate dielectric layer, formed over the substrate, covering the scan line and the gate electrode;
a channel layer, formed over the gate dielectric layer and located over the gate electrode;
a source region, formed on the channel layer, wherein the source region is over a region outside the notch of the gate electrode and the source region overlaps a portion of the gate electrode;

a drain region, formed over the channel layer exposed by the source region, wherein the drain region is over the notch of the gate electrode and the drain region overlaps a portion of the gate electrode at the edge of the notch;
a data line, formed on the gate dielectric layer, wherein the data line is electrically connected to the source region;
a protection layer, formed over the substrate, covering the gate electrode, the gate dielectric layer, the channel layer, the source region, the drain region, the scan line and the data line;
a contact, formed within the protection layer and electrically connected to the drain region; and
a pixel electrode, formed on the protection layer, the pixel electrode electrically connected to the drain region through the contact.

[c8] 8. The pixel structure of claim 7, further comprising an etch stop layer formed between the channel layer and the source and drain regions.

[c9] 9. The pixel structure of claim 7, further comprising an ohmic-contact layer formed between the channel layer and the source and drain regions.

[c10] 10. The pixel structure of claim 7, wherein the source region overlaps the gate electrode.

[c11] 11. The pixel structure of claim 7, wherein the source region comprises two strip regions, each of the two strip regions adjacent to each longitude of the drain region.

[c12] 12. The pixel structure of claim 11, wherein the source region further extends over the gate dielectric layer formed on the scan line.

[c13] 13. The pixel structure of claim 7, wherein the shape of the notch of the gate electrode is a triangle, a quadrilateral or a non-regular shape.

[c14] 14. A thin film transistor, comprising:
a scan line, formed on a substrate;
a gate electrode, formed on the substrate and electrically connected to the scan line, wherein the gate electrode has at least one notch;
a gate dielectric layer, formed over the substrate, covering the scan line and the gate electrode;
a drain region, formed over the notch of the gate electrode and the drain region overlapping a portion of the gate electrode at the edge of the notch and a portion of scan line;
a trident source region, formed on the gate dielectric layer, wherein the trident source region comprises:
two first projecting portions formed on the gate dielec-

tric layer, wherein the two first projecting portions are over a region outside the notch of the gate electrode and the two first projecting portions overlap a portion of the gate electrode;

a second projecting portion, formed over the scan line between the two first projecting portions, wherein the second projecting portion is shorter than the two first projecting portions; and

a connection portion, connecting the second projecting portion and the two first projecting portions; and

a channel layer, formed between the gate electrode and the drain and trident source regions.

[c15] 15. The thin film transistor of claim 14, further comprising an etch stop layer formed between the channel layer and the drain and trident regions.

[c16] 16. The thin film transistor of claim 14, further comprising an ohmic-contact layer formed between the channel layer and the drain and trident source regions.

[c17] 17. The thin film transistor of claim 14, wherein the connection portion of the trident source region extends over the scan line.

[c18] 18. The thin film transistor of claim 14, wherein the shape of the notch of the gate electrode is a triangle, a

quadrilateral or a non-regular shape.

[c19] 19. The thin film transistor of claim 14, further comprising a data line formed on the gate dielectric layer, the data line electrically connected to the trident source region.